



2. (Original) The method as in claim 1, further comprising the step of storing the first sequence of packet data octets in the alignment register when the octet length of the first sequence of packet data octets is less than the octet length of a data word.

3. (Original) The method as in claim 1, further comprising the steps of:  
concatenating at least one packet data octet from a second data word accessed from memory with the second subset of packet data octets stored in the alignment register to generate a second sequence of packet data octets having a octet length at least as great as the octet length of a data word;  
storing the second sequence of packet data octets in the FIFO buffer when the octet length of the sequence of packet data octets is equal to the octet length of a data word; and

storing a first subset of packet data octets from the second sequence of packet data octets in the FIFO buffer and storing a remaining second subset of packet data octets from the second sequence the alignment register when the octet length of the second sequence of packet data octets exceeds the octet length of a data word, wherein an octet length of the first subset of packet data octets of the second sequence is equal to the octet length of a data word.

4. (Original) The method as in claim 1, wherein the octet length of a data word is an integer multiple of four.

5. (Original) A system for transferring network packet data stored in memory to an output device, the system comprising:

    a direct memory access (DMA) interface for accessing a set of data words stored in memory, each data word having at least one valid octet to be included in a network packet and each data word being accessed using a DMA address associated with the data word;

    a first in-first out (FIFO) buffer for storing network packet data to be transmitted by the output device; and

    an alignment block having at least one alignment register, wherein the alignment register for storing at least one data octet, and wherein the alignment block is adapted to:

        concatenate one or more packet data octets from at least a first data word having at least one packet data octet to be included in a network packet to generate a first sequence of packet data octets having an octet length at least as great as an octet length of a data word;

        store the first sequence of packet data octets in a FIFO buffer operably connected to the output device when the octet length of the sequence of packet data octets is equal to the octet length of a data word; and

        store a first subset of packet data octets from the first sequence of packet data octets in the FIFO buffer and storing a remaining second subset of packet data octets from the first sequence in an alignment register when the octet length of the first sequence of packet data octets exceeds the octet length of a data

word, wherein an octet length of the first subset of packet data octets is equal to the octet length of a data word.

6. (Original) The system as in claim 5, wherein the alignment block is further adapted to store the first sequence of packet data octets in the alignment register when the octet length of the first sequence of packet data octets is less than the octet length of a data word.

7. (Original) The system as in claim 5, wherein the alignment block is further adapted to:

concatenate at least one packet data octet from a second data word accessed from memory with the second subset of packet data octets stored in the alignment register to generate a second sequence of packet data octets having a octet length at least as great as the octet length of a data word;

store the second sequence of packet data octets in the FIFO buffer when the octet length of the sequence of packet data octets is equal to the octet length of a data word; and

store a first subset of packet data octets from the second sequence of packet data octets in the FIFO buffer and storing a remaining second subset of packet data octets from the second sequence the alignment register when the octet length of the second sequence of packet data octets exceeds the octet length of a data word, wherein an octet length of the first subset of packet data octets of the second sequence is equal to the octet length of a data word.

8. (Original) The system as in claim 5, wherein the octet length of a data word is an integer multiple of four.

9. (Original) The system as in claim 5, wherein the alignment block further includes at least one FIFO register and is further adapted to store at least a third sequence of one or more packet data octets from a processor in the FIFO register.

10. (Original) The system as in claim 9, wherein the alignment block is further adapted to store the third sequence of packet data octets in the FIFO buffer when an octet length of the third sequence is equal to the octet length of a data word.

11. (Original) The system as in claim 9, wherein the alignment block is further adapted to concatenate at least a subset of the third sequence of packet data octets with a sequence of packet data octets stored in the alignment register to generate a fourth sequence of packet data octets and store the fourth sequence of packet data octets in the FIFO buffer when an octet length of the fourth sequence is equal to the octet length of a data word.

12. (Original) The system as in claim 9, wherein the alignment block is further adapted to concatenate at least a subset of the third sequence of packet data octets with a sequence of packet data octets stored in the alignment register to generate a fourth sequence of packet data octets and store a first subset the fourth sequence of

packet data octets in the FIFO buffer and a remaining second subset of the fourth sequence of packet data octets in the alignment register when an octet length of the fourth sequence exceeds the octet length of a data word.

13. (Original) The system as in claim 9, wherein the alignment block is further adapted to concatenate at least a subset of the third sequence of packet data octets with a sequence of packet data octets stored in the alignment register to generate a fourth sequence of packet data octets and store the fourth sequence of packet data octets in the alignment register when an octet length of the fourth sequence is less than the octet length of a data word.